

Any additional fee required has been calculated as follows:

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	Additional Fee
Total	22	- 24* =		X	
Independent	3	- 3** =		X	
First presentation of Multiple Dependent Claim(s) (if applicable)					
TOTAL					0.00

*not less than 20

** not less than 3

No additional fee is required.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2215.

CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 CFR 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 CFR 1.135. The fee under 37 CFR 1.17 should be charged to our Deposit Account No. 50-2215.

AMENDMENTS TO THE CLAIMS

1. (Canceled)
2. (Previously Presented) The arrangement as claimed in claim 23, wherein the first semiconductor chip is a program-controlled unit.
3. (Previously Presented) The arrangement as claimed in claim 23, wherein the second semiconductor chip is a power chip.
4. (Previously Presented) The arrangement as claimed in claim 23, wherein the second data line is part of a second transmission channel which comprises:
 - a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;
 - the second data line, via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal; and
 - a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line.
5. (Canceled)
6. (Currently Amended) The arrangement as claimed in claim ~~[[5]]~~ 23, wherein the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a pilot data frame or no data.
7. (Original) The arrangement as claimed in claim 6, wherein the first semiconductor chip transmits no further load control data frame for a respective length

of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement.

8. (Original) The arrangement as claimed in claim 7, wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted.

9. (Original) The arrangement as claimed in claim 6, wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

10. (Previously Presented) The arrangement as claimed in claim 23, wherein the first data line is part of a first transmission channel, and the first data line is used to transmit neither load control data nor pilot data.

11. (Previously Presented) The arrangement as claimed in claim 23, wherein the diagnostic data are transmitted in synch with a transmission clock signal generated in the second semiconductor chip, and wherein this transmission clock signal is not transmitted to the first semiconductor chip.

12. (Previously Presented) The arrangement as claimed in claim 23, wherein the first semiconductor chip transmits appropriate pilot data in order to prescribe to the second semiconductor chip what transmission rate is to be used by the second semiconductor chip to transmit the diagnostic data to the first semiconductor chip.

13. (Original) The arrangement as claimed in claim 12, wherein the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant signal.

14. (Original) The arrangement as claimed in claim 13, wherein the transmission clock signal supplied to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

15. (Original) The arrangement as claimed in claim 11, wherein the diagnostic data are transmitted in units of frames, where a frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

16. (Original) The arrangement as claimed in claim 11, wherein the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

17. (Previously Presented) The arrangement as claimed in claim 23, wherein the first data line is part of a first transmission channel comprising a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip, or the second semiconductor chip transmits a transmission clock signal to the first semiconductor chip, and wherein the second semiconductor chip transmits the diagnostic data in synch with this transmission clock signal.

18. (Previously Presented) The arrangement as claimed in claim 23, wherein the second line is part of a second transmission channel which further comprises:

a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a second transmission clock line via which the first semiconductor chip transmits a complementary transmission clock signal to the second semiconductor chip;

a third data line via which the first semiconductor chip transmits complementary load control data and complementary pilot data to the second semiconductor chip; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line.

19. (Previously Presented) The arrangement as claimed in claim 18, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers whose use limits electromagnetic interference.

20. (Previously Presented) The arrangement as claimed in claim 23, wherein the first semiconductor chip has a plurality of respective different output drivers for outputting the load control data, the pilot data and a transmission clock signal, and wherein a user of the arrangement is able to set which of the plurality of different output drivers needs to be used in each case.

21. (Canceled)

22. (Currently Amended) The arrangement as claimed in claim [[5]] 23, wherein the first semiconductor chip is connected to a plurality of second semiconductor chips, every second semiconductor chip is connected to the first semiconductor chip via a dedicated chip select line, and chip select signals transmitted via the chip select lines can be altered during transmission of a frame.

23. (Currently Amended) An arrangement comprising:
a first semiconductor chip; and
a plurality of second semiconductor chips which are connected to and drives electrical loads based on a timing defined by load control data;
a first data line via which the second semiconductor chip transmits diagnostic data, which represent at least one of states prevailing in and events

occurring ~~occurring~~ in the second semiconductor chip, to the first semiconductor chip;
and

a single, second data line via which the first semiconductor chip transmits the load control data and pilot data which control the second semiconductor chips;

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip.

24. (Previously Presented) An arrangement comprising:

a first semiconductor chip; and

a plurality of second semiconductor chips which are connected to and drives electrical loads based on a timing defined by load control data;

a first data communication means for the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, to the first semiconductor chip; and

a single, second data communication means for the first semiconductor chip transmitting the load control data and pilot data which control the second semiconductor chip,

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip.

25. (Currently Amended) A method for communicating in an arrangement having a first semiconductor chip and a plurality of second semiconductor

chips which are connected to and drives electrical loads based on a timing defined by load control data, comprising:

the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring ~~occurring~~ in the second semiconductor chip, via a first data line to the first semiconductor chip; and

the first semiconductor chip transmitting the load control data and pilot data, which control the second semiconductor chips, via a single, second data line,

wherein the load control data and the pilot data are transmitted in units of frames, and wherein the load control data frames and the pilot data frames are transmitted using time-division multiplexing; and

wherein a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip.